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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO
10/770,479	02/04/2004	Masaki Ito	NITT.0189	1890
7590 05/18/2005			EXAMINER	
REED SMITH LLP Suite 1400 3110 Fairview Park Drive Falls Church, VA 22042			THOMPSON, ANNETTE M	
			ART UNIT	PAPER NUMBER
			_ 2825	
			DATE MAILED: 05/18/2005	

Please find below and/or attached an Office communication concerning this application or proceeding.

		Application No.	Applicant(s)			
Office Action Summary		10/770,479	ITO, MASAKI			
		Examiner	Art Unit			
		A. M. Thompson	2825			
The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply						
THE - Exte after - If the - If NO - Failu Any	ORTENED STATUTORY PERIOD FOR REPLY MAILING DATE OF THIS COMMUNICATION. nsions of time may be available under the provisions of 37 CFR 1.13 SIX (6) MONTHS from the mailing date of this communication. a period for reply specified above is less than thirty (30) days, a reply period for reply is specified above, the maximum statutory period were to reply within the set or extended period for reply will, by statute, reply received by the Office later than three months after the mailing ed patent term adjustment. See 37 CFR 1.704(b).	36(a). In no event, however, may a reply be timed within the statutory minimum of thirty (30) days fill apply and will expire SIX (6) MONTHS from cause the application to become ABANDONE!	nely filed s will be considered timely. the mailing date of this communication. D (35 U.S.C. § 133).			
Status		•				
1)⊠	1) Responsive to communication(s) filed on 04 February 2005.					
2a)⊠	This action is <b>FINAL</b> . 2b) ☐ This	action is non-final.				
3)□	Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.					
Disposit	ion of Claims					
5)□ 6)⊠	<u>,                                     </u>					
Applicati	ion Papers					
9)[	The specification is objected to by the Examiner	r.				
10) The drawing(s) filed on is/are: a) accepted or b) objected to by the Examiner.						
	Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).					
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.						
Priority ι	ınder 35 U.S.C. § 119					
12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  a) ☐ All b) ☐ Some * c) ☒ None of:  1. ☒ Certified copies of the priority documents have been received.  2. ☐ Certified copies of the priority documents have been received in Application No  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  * See the attached detailed Office action for a list of the certified copies not received.						
Attachmen	t(s)					
	e of References Cited (PTO-892)	4) Interview Summary				
3) 🔲 Infor	e of Draftsperson's Patent Drawing Review (PTO-948) nation Disclosure Statement(s) (PTO-1449 or PTO/SB/08) r No(s)/Mail Date	Paper No(s)/Mail Da 5) Notice of Informal Pa 6) Other:	te atent Application (PTO-152)			

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## **DETAILED ACTION**

Applicant's amendment to application, 10/770,479, has been examined. Claims 1, 4, and 5 are amended. Claims 6 and 7 are added. Claims 1-7 are pending.5 are pending.

#### **Priority**

1. Acknowledgment is made of applicant's claim for foreign priority based on an application filed in Japan on 06/02/2001. It is noted, however, that applicant has not filed, either with the instant application or with the parent application a certified copy of the Japanese application as required by 35 U.S.C. 119(b).

#### Information Disclosure Statement

2. The foreign patent document listed on Applicant's PTO-1449 has not been considered because it has not been provided with the Applicant's filing and a concise explanation of its relevance is not included.

#### Claim Rejections - 35 USC § 112

- 3. The following is a quotation of the first paragraph of 35 U.S.C. 112:
  - The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.
- 4. Claim 6 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Applicant's limitation of an interface checker incorporated into the semiconductor

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integrated circuit device for logic synthesis and verification is unsupported by Applicant's specification.

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claim 7 is rejected under 35 U.S.C. 112, second paragraph, as failing to set forth the subject matter which applicant(s) regard as their invention. Pursuant to claim 7, Applicant's limitation of generating and verifying a logic model of the semiconductor integrated circuit, while a part of the Invention background, is unsupported by the sections of the specification that discloses Applicant's invention and it is therefore unclear whether such a step is part of Applicant's invention.

## Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

## Rejection of claims 1-5

8. Claims 1-5 are rejected under 35 U.S.C. 102(e) as being anticipated by Rajsuman et al. (Rajsuman), U.S. Patent 6,678,645. Rajsuman discloses a method and apparatus for SOC design validation.

- 9. Pursuant to claim 1, Rajsuman discloses a semiconductor integrated circuit device (Abstract, Figure 3) comprising first and second circuit blocks (Fig. 3, #41, A, B, C); an interface checker which is installed on the semiconductor circuit and monitors whether waveforms of signals between the first and second circuit blocks conform to an interface specification of a design data of the first circuit block (see also col. 10, II. 52-65; col. 5, II. 16-30); and an external output pin to output a result of a monitoring of the interface checker to an external of the semiconductor IC device (Fig. 3).
- 10. Pursuant to claim 2 wherein the external output pin outputs a value indicating conformity or non-conformity (col. 7, II. 60-65, the response comparison).
- 11. Pursuant to claim 3, wherein the interface specification describes timing information in synchronization with a clock signal (col. 10, II. 4-40).
- 12. Pursuant to claim 4, Rajsuman discloses a method (Abstract) that provides design data and an interface specification of the design data; generates a synthesizable interface checker in accordance with the specification (col. 10, line 40 to col. 11, line 27); producing a semiconductor IC including a first logic circuit (col. 6, II. 33-56); using the installed interface checker to monitor whether waveforms of signals between circuit blocks conform to an interface specification (col. 9, line 34 to col. 10, line 39, the verification unit; see also col. 10, II. 53-65).

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13. Pursuant to claim 5, further comprising outputting a first value indicating a conformity of the waveforms to the interface specification or a second value indicating a nonconformity of the waveforms to the interface specification outside of the semiconductor IC (col. 7, II. 60-65, the response comparison).

#### Remarks

14. Applicant's added limitation of an interface checker that is part of or installed on the semiconductor device is already disclosed by Rajsuman (col. 10, lines 52-65). Therefore the claim rejections are maintained.

### Conclusion

15. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

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Any inquiry concerning this communication or earlier communications should be 16. directed to Examiner A.M. Thompson whose telephone number is (571) 272-1909. The

Examiner can usually be reached Monday thru Friday from 8:00 a.m. to 4:30 p.m..

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

17. Responses to this action should be mailed to the appropriate mail stop:

Mail Stop

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

or faxed to:

(703) 872-9306, (for all **OFFICIAL** communications intended for entry)

Primary Examiner

Technology Center 2800